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| EXAMINER | |
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| LAMARRE, GUY J | |
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

| SUPPLEMENTAL **Notice of Allowability** | **Application No.** 10/733,645 | **Applicant(s)** LIMBERG, ALLEN LEROY | |
|---|---|---|---|
| | **Examiner** Guy J. Lamarre | **Art Unit** 2133 | |

***-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--***

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *8/05/04*.

2. ☒ The allowed claim(s) is/are *1-75*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS ( as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review ( PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   **Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).**

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *1/23/07* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Guy J. Lamarre, P.E.
Primary Examiner

## Examiner's Amendment & Reasons For Allowance

### Examiner's Amendment

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

The following has been amended:

a) **Claim 39 is replaced as follows:**

The method of claim 36, wherein said still other data packets used in said step (f) of time-division multiplexing consist of MPEG-2-compliant 187-byte data packets, and wherein the method of claim 36 further includes a step of: (k) randomizing each of said still other data packets throughout all of its portions.

b) **Claim 71 is replaced as follows:**

The receiver of claim 70, wherein said error-correction circuitry comprises:

a first decoder for lateral Reed-Solomon forward-error-correction coding, connected for correcting said successive segments of said de-interleaver response to generate respective successive segments of a de-interleaver response with initial lateral Reed-Solomon error-correction;

a second decoder for lateral Reed-Solomon forward-error-correction coding, connected for supplying said successive segments of said error-corrected randomized baseband digital signal to said first data de-randomizer;

a plurality of decoders for transverse Reed-Solomon forward-error-correction coding;

Reed-Solomon forward-error-correction decoder application circuitry connected for selecting one of said plurality of decoders for transverse Reed-Solomon

forward-error-correction coding to be used in transverse Reed-Solomon forward-error-correction decoding operations; and

random-access memory for temporarily storing in respective first and second banks thereof respective super groups of successive data segments extracted from said de-interleaver response with initial lateral Reed-Solomon error-correction,

said first and second banks of said random-access memory connected for successive cycles of read-then-write-over operation, which cycles are considered for purposes of claiming to be ordinally numbered in order of their occurrence in time, said first bank of said random-access memory connected for having each successive segment of the super group temporarily stored therein laterally scanned during odd-numbered cycles of read-then-overwrite operation for reading to said second decoder for lateral Reed-Solomon forward-error-correction coding and for then being overwritten by a fresh segment of said de-interleaver response with initial lateral Reed-Solomon error-correction supplied from said first decoder for lateral Reed-Solomon forward-error-correction coding, said first bank of said random-access memory connected for having the super group temporarily stored therein transversely scanned during even-numbered cycles of read-then-overwrite operation for reading to the one of said plurality of decoders for transverse Reed-Solomon forward-error-correction coding selected by said Reed-Solomon forward-error-correction decoder application circuitry to be used in transverse Reed-Solomon forward-error-correction decoding operations and for then being overwritten by corrected transverse Reed-Solomon forward-error-correction coding from said decoder so selected, said second bank of said random-access memory connected for having each successive segment of the super group temporarily stored therein laterally scanned during even-numbered cycles of

read-then-overwrite operation for reading to said second decoder for lateral Reed-Solomon forward-error-correction coding and for then being overwritten by a fresh segment of said de-interleaver response with initial lateral Reed-Solomon error-correction supplied from said first decoder for lateral Reed-Solomon forward-error-correction coding, said second bank of said random-access memory connected for having the super group temporarily stored therein transversely scanned during odd-numbered cycles of read-then-overwrite operation for reading to the one of said plurality of decoders for transverse Reed-Solomon forward-error-correction coding selected by said Reed-Solomon forward-error-correction decoder application circuitry to be used in transverse Reed-Solomon forward-error-correction decoding operations and for then being overwritten by corrected transverse Reed-Solomon forward-error-correction coding from said decoder so selected.

c) **Claims 72-75 are added as follows:**

72. The receiver of claim 71, further comprising:

a transmission mode detector responsive to selected portions of said baseband digital signal for determining which if any of said plurality of decoders for transverse Reed-Solomon forward-error-correction coding is to be employed and for controlling said Reed-Solomon forward-error-correction decoder application circuitry in its selection of one of said plurality of decoders for transverse Reed-Solomon forward-error-correction coding to be used in said transverse Reed-Solomon forward-error-correction decoding operations.

73. The receiver of claim 72, further comprising:

a second data de-randomizer connected for de-randomizing at least the randomized packet identifier (PID) bits in each of said successive segments of said de-interleaver response

with initial lateral Reed-Solomon error-correction generated by said first decoder for lateral Reed-Solomon forward-error-correction coding, said transmission mode detector being connected to receive the de-randomized PID bits for use in determining which if any of said plurality of decoders for transverse Reed-Solomon forward-error-correction coding is to be employed.

74. The receiver of claim 49, wherein said trellis decoder is of a plural-mode type capable of selectively demodulating symbols transmitted using a full 8VSB alphabet and symbols transmitted using a restricted 8VSB alphabet, said receiver further comprising:

first, second and third packet decoders, said first packet decoder being of MPEG-2 type for use in decoding video data packets, and said second packet decoder being of AC-3 type for use in decoding audio data packets;

a transport stream de-multiplexer connected for receiving said transport stream from said first data de-randomizer, for sorting video data packets from said transport stream to said first packet decoder, and for sorting audio data packets from said transport stream to said second packet decoder;

a first 2-segments-to-1 data compressor connected for receiving pairs of data packets that include 184-byte portions demodulated from symbols transmitted using said restricted 8VSB alphabet, said 2-segments-to-1 data compressor reproducing in its response to each said pair of data packets a respective single randomized data packet; and

a second data de-randomizer connected for receiving as its input signal the response of said first 2-segments-to-1 data compressor and responding to said randomized data packets in that response to supply de-randomized data packets to said third packet decoder as input signal thereto.

75. The receiver of claim 74 wherein said error-correction circuitry comprises:

first, second and third decoders for lateral Reed-Solomon forward-error-correction coding, said first decoder for lateral Reed-Solomon forward-error-correction coding connected for correcting said successive segments of said de-interleaver response to generate respective successive segments of a de-interleaver response with initial lateral Reed-Solomon error-correction, said second decoder for lateral Reed-Solomon forward-error-correction coding connected for supplying said successive segments of said error-corrected randomized baseband digital signal to said first data de-randomizer, said third decoder for lateral Reed-Solomon forward-error-correction coding connected for supplying said first 2-segments-to-1 data compressor its input signal composed of pairs of randomized data packets;

a second 2-segments-to-1 data compressor connected for receiving pairs of data segments from said error-corrected randomized baseband digital signal supplied by said second decoder for lateral Reed-Solomon forward-error-correction coding, which pairs of data segments include 184-byte packets demodulated from symbols transmitted using said restricted 8VSB alphabet, said second 2-segments-to-1 data compressor reproducing in its response to each said pair of data segments a respective single extended data segment, the extended data segments in the response of said 2-segments-to-1 data compressor at times being subject to transversal Reed-Solomon forward-error-correction coding;

circuitry for expanding each of extended data segments into a respective pair of data segments, which said third decoder for lateral Reed-Solomon forward-error-correction coding is connected to receive as input signal thereto;

a plurality of decoders for transverse Reed-Solomon forward-error-correction coding;

first Reed-Solomon forward-error-correction decoder application circuitry connected for selecting one of said plurality of decoders for transverse Reed-Solomon forward-error-correction coding to be used in first transverse Reed-Solomon forward-error-correction decoding operations;

second Reed-Solomon forward-error-correction decoder application circuitry connected for selecting one of said plurality of decoders for transverse Reed-Solomon forward-error-correction coding to be used in second transverse Reed-Solomon forward-error-correction decoding operations;

a first random-access memory for temporarily storing in respective first and second banks thereof respective super groups of data segments extracted from said de-interleaver response with initial lateral Reed-Solomon error-correction, said first and second banks of said first random-access memory connected for successive cycles of read-then-write-over operation used in said first transverse Reed-Solomon forward-error-correction decoding operations, which cycles are considered for purposes of claiming to be ordinally numbered in order of their occurrence in time,

said first bank of said first random-access memory connected for having each successive segment of the super group temporarily stored therein laterally scanned during odd-numbered cycles of read-then-overwrite operation for reading to said second decoder for lateral Reed-Solomon forward-error-correction coding and for then being overwritten by a fresh segment of said de-interleaver response with initial lateral Reed-Solomon error-correction, said first bank of said first random-access memory connected for having the super group temporarily stored therein transversely scanned during even-numbered cycles of read-then-overwrite operation for reading to the one of said plurality of decoders for transverse Reed-Solomon forward-error-correction coding selected to be used in said first transverse Reed-

Solomon forward-error-correction decoding operations and for then being overwritten by corrected transverse Reed-Solomon forward-error-correction coding from said decoder selected to be used in said first transverse Reed-Solomon forward-error-correction decoding operations, said second bank of said first random-access memory connected for having each successive segment of the super group temporarily stored therein laterally scanned during even-numbered cycles of read-then-overwrite operation for reading to said second decoder for lateral Reed-Solomon forward-error-correction coding and for then being overwritten by a fresh segment of said de-interleaver response with initial lateral Reed-Solomon error-correction, said second bank of said first random-access memory connected for having the super group temporarily stored therein transversely scanned during odd-numbered cycles of read-then-overwrite operation for reading to the one of said plurality of decoders for transverse Reed-Solomon forward-error-correction coding selected to be used in said first transverse Reed-Solomon forward-error-correction decoding operations and for then being overwritten by corrected transverse Reed-Solomon forward-error-correction coding from said decoder selected to be used in said first transverse Reed-Solomon forward-error-correction decoding operations; and

a second random-access memory for temporarily storing in respective first and second banks thereof respective super groups of extended data segments extracted from the response of said 2-segments-to-1 data compressor, said first and second banks of said second random-access memory connected for successive cycles of read-then-write-over operation used in said second transverse Reed-Solomon forward-error-correction decoding operations, which cycles are considered for purposes of claiming to be ordinally numbered in order of their occurrence in time, said first bank of said second random-access memory connected for having each successive extended data segment of the super group temporarily stored therein laterally scanned during

odd-numbered cycles of read-then-overwrite operation for reading to said circuitry for expanding each of extended data segments into a respective pair of data segments and for then being overwritten by a fresh extended data segment from the response of said second 2-segments-to-1 data compressor, said first bank of said second random-access memory connected for having the super group temporarily stored therein transversely scanned during even-numbered cycles of read-then-overwrite operation for reading to the one of said plurality of decoders for transverse Reed-Solomon forward-error-correction coding selected to be used in said second transverse Reed-Solomon forward-error-correction decoding operations and for then being overwritten by corrected transverse Reed-Solomon forward-error-correction coding from said decoder selected to be used in said second transverse Reed-Solomon forward-error-correction decoding operations, said second bank of said second random-access memory connected for having each successive segment of the super group temporarily stored therein laterally scanned during even-numbered cycles of read-then-overwrite operation for reading to said circuitry for expanding each of extended data segments into a respective pair of data segments and for then being overwritten by a fresh extended data segment from the response of said second 2-segments-to-1 data compressor, said second bank of said second random-access memory connected for having the super group temporarily stored therein transversely scanned during odd-numbered cycles of read-then-overwrite operation for reading to the one of said plurality of decoders for transverse Reed-Solomon forward-error-correction coding selected to be used in said second transverse Reed-Solomon forward-error-correction decoding operations and for then being overwritten by corrected transverse Reed-Solomon forward-error-correction coding from said decoder selected to be used in said second transverse Reed-Solomon forward-error-correction decoding operations.

**Reasons For Allowance**

**2.** **Claims 1-75** are allowable over the prior art.

**2.1** The following is an Examiner's statement of reasons for the indication of allowable subject matter: the prior art is exemplified by **Limberg et al.** (US Patent Nos. 6426780; 6496230) and **Wan et al.** (US Patent No. 6430159).

**For example, Limberg et al.** (US Patent No. 6426780) discloses data processing with error correction capability comprising data coding procedure wherein: ' *symbol decoder 16 supplies symbol decoding results in 3-parallel-bit groups, assembled by a data assembler 17 for application to trellis decoder circuitry 18. Trellis decoder circuitry 18 conventionally uses twelve trellis decoders. The trellis decoding results are supplied from the trellis decoder circuitry 18 to byte de-interleaver circuitry 19. Byte de-interleaver circuitry 19 parses the trellis decoding results into bytes and performs diagonal byte interleaving over a prescribed portion of the data field to recover bytes of Reed-Solomon error-correction coding for application to Reed-Solomon decoder circuitry 20. Reed-Solomon decoding by the circuitry 20 generates an error-corrected byte stream supplied to a data de-randomizer 21. The data de-randomizer 21 supplies reproduced data to the remainder of the receiver (not shown). The remainder of a complete DTV receiver will include a packet sorter, an audio decoder, an MPEG-2 decoder and so forth. The remainder of a DTV signal receiver incorporated in a digital tape recorder/reproducer will include circuitry for converting the data to a form for recording.*'

**However, these references** do not teach or suggest the combination of claim elements described in **Claims 1-75**.

**2.2** Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

## Conclusion

* Any response to this action should be mailed to:

Commissioner of Patents and Trademarks, Washington, D.C. 20231

**or faxed to:** (571) 273-8300 for all formal communications.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Guy J. Lamarre, P.E., whose telephone number is (571) 272-3826. The examiner can normally be reached on Monday to Friday from 9:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert De Cady, can be reached at (571) 272-3819.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-3609.

Information regarding the status of an application may also be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Guy J. Lamarre, P.E
Primary Examiner
1/23/2007